Lab 3

ECE 3300 LAB

SECTION 02

Instructor: Mohamed Aly

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Group I

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**Abstract**

Purpose of the experiment was to create a variable clock divider on the Arty 7 FPGA board. Task was to create 4x16 decoder by instantiation. One button would be used to reset the clock speed. Decoder was created using structural modeling. From there, the high frequencies would make the LED flash at a fast paced while low frequencies would be slower.

**Theory: Sketch of Design**

A picture containing diagram

Description automatically generated

**Area/Resources Information**

Elaborated Design

Graphical user interface, chart, table

Description automatically generated with medium confidence

**Power Usage**

**Graphical user interface

Description automatically generated**

**Post-Implementation Resource Utilization**

